

Anusha S Gouda

Design Verification Engineer, anushag695@gmail.com

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CAREER OBJECTIVE

Aspiring Design Verification Engineer with training in SystemVerilog and UVM, including AXI and APB protocol verification. Skilled in UVM testbench development, constrained-random verification, System Verilog Assertions (SVA), and functional coverage. Seeking an entry-level VLSI Design Verification role to contribute to ASIC/SoC verification.

PROFESSIONAL TRAINING

Advanced Design and Verification Trainee - Maven Silicon

July 2025 -present

Gained hands-on training in SystemVerilog and UVM-based ASIC verification Developed testbenches for AXI and APB protocol verification environments Worked on assertions, functional coverage, and structured verification components

EDUCATION

Canara Engineering College

Bachelor of Engineering in Electronics and Communication Engineering

Nov 2021 - June 2025

(CGPA of 8.64)

Konkan PU College

Department of Pre-University Education Board

Aug 2019 - July 2021

(Percentage - 93.5%)

New English School

Karnataka Secondary Education Examination board

June 2018 – March 2019

(Percentage - 92.96%)

SKILLS

HDL: Verilog

HVL: SystemVerilog

Protocol: AXI, APB, SPI

Verification Methodology: Constraint-Random Coverage Driven Verification

Assertion Based Verification: SVA

TB Methodology: UVM

EDA Tool: VCS, Mentor Graphics-Quarta Sim, Xilinx-ISE, Synopsys Design compiler, VC Spyglass Lint

Core Skills: RTL coding using Synthesizable constructs of Verilog, FSM based design, Simulation, Functional Coverage

PROJECTS

AXI VIP-Based Verification Project

Apr 2026 - Apr 2026

Tools used - QuestaSim/ModelSim, VCS.

- Developed a UVM-based verification environment using AXI VIP for AXI protocol verification.
- Integrated Master and Slave VIPs for read/write channel verification and implemented constrained-random stimulus with functional coverage. Verified protocol compliance across FIXED, INCR, and WRAP burst types.

APB-Based SPI Master Controller (Design and Verification) Dec 2025 - Jan 2026 Tools

used - Xilinx ISE, Design Compiler, QuestaSim/ModelSim, VCS.

- Designed an SPI Master controller with APB interface using Verilog HDL. Developed UVMbased testbench to verify APB Based SPI Protocol.
- Implemented SystemVerilog Assertions and functional coverage to verify APB/SPI protocol behavior.

INTERNSHIP

Design Thinking and Prototyping By Kakunje Software Private Limited | Mar 2024 - May 2024

- Gained exposure to PCB design using Ki-CAD EDA tool.
- Designed basic electronic circuits and contributed to prototype development.

Training On C Programming ,Data Structure and Soft Skills by Qspiders | July 2023 - Sep 2023

- Strengthen understanding of C fundamentals, data structures, and problem-solving techniques.
- Improved communication and presentation skills through soft skill sessions.

SOFT SKILLS

- Effective communication
- Problem-solving
- Leadership, Critical Thinking

CERTIFICATIONS

- **VLSI SoC** : Completed VLSI Soc Design course and VLSI System on Chip design using Verilog HDL by MAVEN SILICON.
- **C and Python Programming** : Taken C and Python Programming courses through SPOKEN TUTORIAL by IIT Bombay.

Date:

place: Bengaluru

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