RAVI PRAKASH YADAV

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SUMMARY

Software engineer with hands-on experience in C/C++, system-level development, debugging, performance optimization, and cross-platform software on Windows and Linux. Experienced in analyzing behavior under varied workloads, building test harnesses, validating throughput and latency, and optimizing data paths that interact with hardware. Focused on reliable, maintainable software and data-driven performance improvements.

SKILLS

Languages: C, C++ (low-latency, lock-free, cache-aware design)

Embedded & Hardware: Embedded Linux, Xilinx/AMD RFSoC, DMA and zero-copy data paths, NIC drivers, FPGA integration testing, ARM Compiler 5 / 6 toolchains

Low-Latency & Systems: Kernel-bypass I/O, lock-free pipelines, multithreading, buffer management, software timestamping, latency profiling, data structures & algorithms

Protocols & Networking: ARQ retransmission (SNACK/SACK), UDP, DPDK, QoS, POSIX sockets, packet-loss / lossy-link tuning, NSE NNF / MTBT

Safety & Quality: MISRA-C, LDRA, DOC-105, code-coverage analysis, end-to-end test harnesses

WORK EXPERIENCE

R&D Engineer I · QbitLabs ***Jul 2024 – Present***

Joined as Intern (Jul 2024); R&D Engineer Trainee (Sep 2024); promoted to R&D Engineer I (Apr 2025). Module owner on DRDO-funded HDR modem.

- Owned the **zero-copy DMA pipeline** and **SNACK/SACK retransmission engine** of the HDR modem for defence satellite links (see Projects).
- **Safety compliance:** Led MISRA-C compliance and code-coverage analysis using LDRA under DOC-105, ensuring production-grade embedded code quality.
- **Toolchain:** Led migration from ARM Compiler 5 to ARM Compiler 6, saving ~$30,000 in licensing costs and eliminating legacy build instability.
- **Debugging:** Resolved cross-platform (Windows/Linux) video codec defects, enabling reliable satellite image transfers exceeding 100 GB.
- **Verification:** Designed and ran end-to-end test harnesses validating throughput, latency and protocol correctness.

PROJECTS

Zero-Copy High-Speed Data Path (Xilinx RFSoC) · HDR Modem *2024–2025*

- Implemented a high-throughput zero-copy DMA pipeline on Xilinx RFSoC, eliminating redundant memory copies and significantly reducing CPU overhead.
- Scaled system bandwidth **20× (50 Mbps → 1 Gbps)** while sustaining low latency under continuous high-throughput load.

HDR Modem Protocol – SNACK/SACK Retransmission Engine *2024–2025*

- Owned the retransmission engine; profiled and tuned it to minimise unnecessary retransmits under varied packet-loss conditions.
- Optimised critical modem data paths, improving latency and reliability across lossy communication links.

NIC Driver & Userspace SDK*2026*

- Built a custom NIC driver and userspace SDK for FPGA integration testing, enabling low-latency packet TX/RX with optimised buffer management and reduced syscall overhead.

Low-Latency Matching Engine & Exchange Simulation *2025 · Solo-built*

- Sole architect and developer; built an NSE-style exchange simulation end-to-end in ~4 months, including the NNF protocol stack (NetIF library, MTBT handler, NNF stream processing) on a concurrent state-machine architecture.
- Engineered a **sub-microsecond (<1 µs)** order-matching core with one-digit microsecond tick-to-trade latency (software timestamping, simulated UDP order flow).
- Built lock-free packet-processing pipelines, replay/recording logic, low-latency structured logging, and a gateway router with client authentication and per-client session state.

EDUCATION

B.Tech, Electronics & Communication Engineering (ECE) ***2020 – 2024***

Delhi Technological University, New Delhi 7.78