

RAVI PRAKASH YADAV

+91 9312305593

| ravi87iino@gmail.com | [LinkedIn](#)

EDUCATION

B.Tech (ECE) 2020–2024 Delhi Technological University, New Delhi **77.8%**

WORK EXPERIENCE

R&D Engineer I **QbitLabs** Jul 2024 – Present

- ▶ Joined as Intern (Jul 2024); progressed to R&D Engineer Trainee and promoted to R&D Engineer I in Apr 2025.
- ▶ Designed and implemented a **zero-copy DMA pipeline (Xilinx RFSoc)**, scaling throughput **20× (50 Mbps → 1 Gbps)** while reducing CPU overhead.
- ▶ Led migration of the project toolchain from ARM Compiler 5 to ARM Compiler 6, delivering **~\$30,000 in licensing cost savings** and eliminating legacy build instability.
- ▶ Led MISRA-C compliance and code-coverage analysis using LDRA tools under **DOC-105 safety standards**, ensuring production-grade code quality.
- ▶ Resolved cross-platform video codec defects across (Windows/Linux), enabling reliable satellite image transfers **exceeding 100 GB**.

PROJECTS

Low-Latency Matching Engine & Exchange Simulation · 2025 · Solo-built

- ▶ Sole architect and developer — built the entire **Low-Latency Matching Engine & Exchange Simulation from scratch** in ~4 months, simulating NSE trading infrastructure end-to-end.
- ▶ Implemented complete **NSE NNF protocol stack**: NetIF library, MTBT handler, NNF stream processing, and concurrent state-machine architecture.
- ▶ Engineered a **sub-microsecond (<1 μs) order-matching engine core** (isolated matcher logic), achieving **one-digit microsecond** tick-to-trade latency using software timestamping under simulated UDP order flow.
- ▶ Built **lock-free packet processing pipelines**, replay/recording logic, and low-latency structured logging.
- ▶ Designed gateway router, secure client authentication, and session-key generation with per-client state management.

NIC Driver & Userspace SDK · 2026

- ▶ Built a **custom NIC driver and userspace SDK**, enabling low-latency packet TX/RX with optimized buffer management and reduced syscall overhead.

HDR Modem Protocol · 2024–2025 · QbitLabs (Module Owner)

- ▶ Owned the **SNACK/SACK retransmission engine**, profiling and tuning it to minimise unnecessary retransmits under varied packet-loss conditions.
- ▶ Optimised critical modem data-paths, achieving measurable improvements in latency and reliability across lossy communication links.
- ▶ Designed and executed end-to-end test harnesses validating throughput, latency, and protocol correctness.

Zero-Copy High-Speed Data Transfer (RFSoc) · 2024–2025 · QbitLabs (Module Owner)

- ▶ Implemented a **High-Throughput Zero-Copy DMA Pipeline (Xilinx RFSoc)**, eliminating redundant memory copies and significantly reducing CPU overhead.
- ▶ Scaled system bandwidth from **50 Mbps to 1 Gbps** while sustaining low-latency performance under continuous high-throughput load.

SKILLS

Technical: C/C++ · Low-Latency Architecture · Lock-Free Concurrency · Embedded Linux · DMA · Networking Protocols · Multithreading · POSIX Sockets · MISRA-C · Data Structures & Algorithms

Tooling & Standards: MISRA-C · LDRA · ARM Compiler Toolchains